CLAIMS

We claim:

1. A method of forming small features, comprising the steps of:

providing a substrate having a dielectric layer formed thereover;

forming a spacing layer over the dielectric layer; the spacing layer having a thickness equal to the thickness of the small feature to be formed;

forming a patterned, re-flowable masking layer over the spacing layer; the masking layer having a first opening with a width "L";

re-flowing the patterned, re-flowable masking layer to form a patterned, re-flowed masking layer having a re-flowed first opening with a lower width "l"; the re-flowed first opening lower width "l" being less than the pre-re-flowed first opening width "L";

etching the spacing layer to the dielectric layer using the patterned, re-flowed masking layer as a mask to form a second opening within the etched spacing layer having a width equal to the re-flowed first opening lower width "l";

removing the patterned, re-flowed masking layer;

forming a small feature material within the second opening;

removing any excess small feature material above the etched spacing layer; and

removing the etched spacing layer to form the small feature comprised of the small feature material.

2. The method of claim 1, wherein the substrate is formed of a material selected from the group consisting of silicon and silicon germanium; the dielectric layer is

formed of a material selected from the group consisting of grown silicon oxide and deposited silicon oxide; the spacing layer is formed of a material selected from the group consisting of silicon nitride and silicon oxynitride; the masking layer is formed of doped oxide; and the small feature material is formed of a material selected from the group consisting of polysilicon, polysilicon germanium (poly SiGe), titanium, molybdenum, nickel and stacks comprised of the above materials.

3. The method of claim 1, wherein the substrate is formed of silicon; the dielectric layer is formed of silicon oxide; the spacing layer is formed of silicon nitride; the masking layer is formed of a doped oxide; and the small feature material is formed of polysilicon.

4. The method of claim 1, wherein the pre-re-flowed first opening width "L" has a width of from about 1000 to 1800Å and the re-flowed first opening lower width "l" has a width of from about 200 to 800Å.

5. The method of claim 1, wherein the pre-re-flowed first opening width "L" has a width of from about 1200 to 1500Å and the re-flowed first opening lower width "l" has a width of from about 250 to 800Å.

6. The method of claim 1, wherein the dielectric layer is from about 15 to 100Å thick; and the masking layer is from about 400 to 2000Å thick.

7. The method of claim 1, wherein the dielectric layer is from about 20 to 50Å thick; and the masking layer is from about 1000 to 1500Å thick.

8. The method of claim 1, including the step of forming a gate dielectric layer liner within the second opening.

9. The method of claim 1, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer being formed of a material selected from the group consisting of silicon oxide, nitrided silicon oxide, a silicon oxide/nitride stack and a high-k dielectric material such as aluminum oxide.

10. The method of claim 1, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer liner having an EOT thickness of from about 7 to 20Å.

11. The method of claim 1, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer liner having an EOT thickness of from about 10 to 16Å.

12. The method of claim 1, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle.

13. The method of claim 1, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle conducted at a temperature of from about 850 to 950°C for from about 900 to 1800seconds.

14. A method of forming small features, comprising the steps of:

providing a substrate having a dielectric layer formed thereover;

forming a spacing layer over the dielectric layer; the spacing layer having a thickness equal to the thickness of the small feature to be formed;

forming a patterned, re-flowable masking layer over the spacing layer; the masking layer having a first opening with a width "L" of from about 1000 to 1800Å;

re-flowing the patterned, re-flowable masking layer to form a patterned, re-flowed masking layer having a re-flowed first opening with a lower width "l" of from about 200 to 800Å;

etching the spacing layer to the dielectric layer using the patterned, re-flowed masking layer as a mask to form a second opening within the etched spacing layer having a width equal to the re-flowed first opening lower width "l";

removing the patterned, re-flowed masking layer;

forming a small feature material within the second opening;

removing any excess small feature material above the etched spacing layer; and

removing the etched spacing layer to form the small feature comprised of the small feature material.

15. The method of claim 14, wherein the substrate is formed of a material selected from the group consisting of silicon and silicon germanium; the dielectric layer is formed of a material selected from the group consisting of grown silicon oxide and deposited silicon oxide; the spacing layer is formed of a material selected from the group consisting of silicon nitride and silicon oxynitride; the masking layer is formed of doped oxide; and the small feature material is formed of a material selected from the group consisting of polysilicon, polysilicon germanium (poly SiGe), titanium, molybdenum, nickel and stacks comprised of the above materials.

16. The method of claim 14, wherein the substrate is formed of silicon; the dielectric layer is formed of silicon oxide; the spacing layer is formed of silicon nitride; the masking layer is formed of a doped oxide; and the small feature material is formed of polysilicon.

17. The method of claim 14, wherein the pre-re-flowed first opening width "L" has a width of from about 1200 to 1500Å and the re-flowed first opening lower width "l" has a width of from about 250 to 800Å.

18. The method of claim 14, wherein the dielectric layer is from about15 to 100Å thick; and the masking layer is from about 400 to 2000Å thick.

19. The method of claim 14, wherein the dielectric layer is from about 20 to 50Å thick; and the masking layer is from about 1000 to 1500Å thick.

20. The method of claim 14, including the step of forming a gate dielectric layer liner within the second opening.

21. The method of claim 14, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer being formed of a material selected from the group consisting of silicon oxide, nitrided silicon oxide, a silicon oxide/nitride stack and a high-k dielectric material such as aluminum oxide.

22. The method of claim 14, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer liner having an EOT thickness of from about 7 to 20Å.

23. The method of claim 14, including the step of forming a gate dielectric layer liner within the second opening; the gate dielectric layer liner having an EOT thickness of from about 10 to 16Å.

24. The method of claim 14, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle.

25. The method of claim 14, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle conducted at a temperature of from about 850 to 950°C for from about 900 to 1800seconds.

26. A method of forming small features, comprising the steps of:

providing a substrate having a dielectric layer formed thereover;

forming a spacing layer over the dielectric layer; the spacing layer having a thickness equal to the thickness of the small feature to be formed;

forming a patterned, re-flowable masking layer over the spacing layer; the masking layer having a first opening with a width "L" of from about 1000 to 1800Å;

re-flowing the patterned, re-flowable masking layer to form a patterned, re-flowed masking layer having a re-flowed first opening with a lower width "l" of from about 200 to 800Å;

etching the spacing layer to the dielectric layer using the patterned, re-flowed masking layer as a mask to form a second opening within the etched spacing layer having a width equal to the re-flowed first opening lower width "l";

removing the patterned, re-flowed masking layer;

forming a gate dielectric layer liner within the second opening

forming a small feature material within the gate dielectric layer lined second opening;

removing any excess small feature material and gate dielectric layer liner above the etched spacing layer; and

removing the etched spacing layer to form the small feature comprised of the small feature material.

27. The method of claim 26, wherein the substrate is formed of a material selected from the group consisting of silicon and silicon germanium; the dielectric layer is formed of a material selected from the group consisting of grown silicon oxide and deposited silicon oxide; the spacing layer is formed of a material selected from the group consisting of silicon nitride and silicon oxynitride; the masking layer is formed of doped oxide; and the small feature material is formed of a material selected from the group consisting of polysilicon, polysilicon germanium (poly SiGe), titanium, molybdenum, nickel and stacks comprised of the above materials.

28. The method of claim 26, wherein the substrate is formed of silicon; the dielectric layer is formed of silicon oxide; the spacing layer is formed of silicon nitride; the masking layer is formed of a doped oxide; and the small feature material is formed of polysilicon.

29. The method of claim 26, wherein the pre-re-flowed first opening width "L" has a width of from about 1200 to 1500Å and the re-flowed first opening lower width "l" has a width of from about 250 to 800Å.

30. The method of claim 26, wherein the dielectric layer is from about15 to 100Å thick; and the masking layer is from about 400 to 2000Å thick.

31. The method of claim 26, wherein the dielectric layer is from about 20 to 50Å thick; and the masking layer is from about 1000 to 1500Å thick.

32. The method of claim 26, wherein the gate dielectric layer is formed of a material selected from the group consisting of silicon oxide, nitrided silicon oxide, a silicon oxide/nitride stack and a high-k dielectric material such as aluminum oxide.

33. The method of claim 26, wherein the gate dielectric layer liner has an EOT thickness of from about 7 to 20Å.

34. The method of claim 26, wherein the gate dielectric layer liner has an EOT thickness of from about 10 to 16Å.

35. The method of claim 26, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle.

36. The method of claim 26, wherein the patterned, re-flowable masking layer is re-flowed by a thermal cycle conducted at a temperature of from about 850 to 950°C for from about 900 to 1800seconds.